

## Instruction Manual

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8900FSS

FRAME SYNCHRONIZER SUBMODULE

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# Preface

## **About This Manual**

This manual describes the features of a specific submodule of the 8900 Series Distribution Amplifier family. As part of this module family, it is subject to Safety and Regulatory Compliance described in the 8900 Series frame and power supply documentation (see the 8900 Series User's Guide).

Preface

# 8900FSS Frame Synchronizer Submodule

### Introduction

The 8900FSS Frame Sync Submodule is a low cost, high density timing solution enabling host signal converter modules to offer infinite frame sync or delay function in the digitized video data stream. The submodule mounts on several host modules in the 8900 Series product line.

#### The 8900FSS features:

- 10-bit signal processing
- Full-frame output phasing
- Multiple frame/field freeze modes
- Autofreeze (hot switch)
- Two reference inputs for multiformat facilities
- Remote control via a frame ethernet interface

#### **Networking Frames**

The 8900FSS submodule networking functions are available when the host module resides in the 8900 Series frames that offer a GUI-based configuration and monitoring system (see *Remote Configuration and Monitoring on page 5.*)

## Installation

To install the 8900FSS submodule on the host module (refer to Figure 1):

- 1. Remove the screw from the outer end of the board spacer post.
- **2.** Carefully attach the 8900FSS to the component side connectors on the host board as shown.

Note The submodule text reading "Front Edge" must be oriented to the Host module front edge (where the card ejector is located). Be certain the mating connector alignment is correct before pressing the submodule into place. Do not force the connection.

**3.** Verify that the spacer post lines up correctly with the hole in the host module. If not, re-examine the connector alignment and submodule orientation. Re-install the screw into the spacer post on the bottom side of the host module.

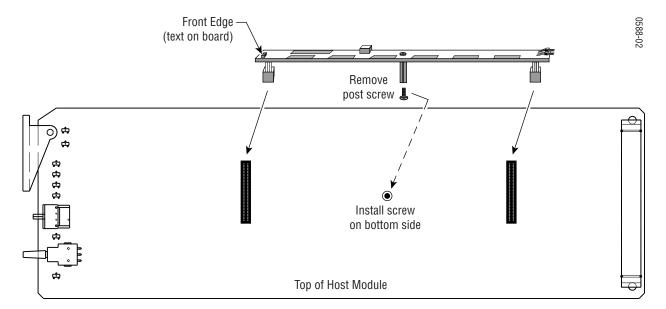


Figure 1. 8900FSS Installation on Host Module

#### **Termination Selection**

Before installing the host module in the frame, verify the correct reference signal termination selection is set using the jumpers JP3 and JP4 on the submodule (see Figure 2). In most applications of the 8900FSS the  $75\Omega$  position is used. Refer to documentation for the host module for the recommended termination selection.

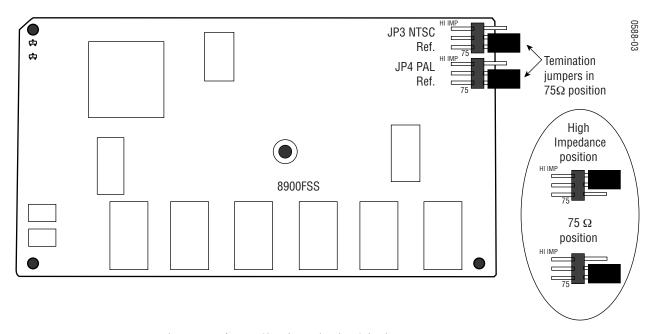


Figure 2. Reference Signal Termination Selection

## **Power Up**

When power is applied to the host module, the 8900FSS will indicate if a reference signal is not present by illuminating the red Error LED. In the factory default configuration the Freeze function is not activated, so the yellow Freeze LED will not illuminate (see *Indicator LEDs on page 4*). The possible LED states and their indicated Input/Output conditions are shown in Table 1.

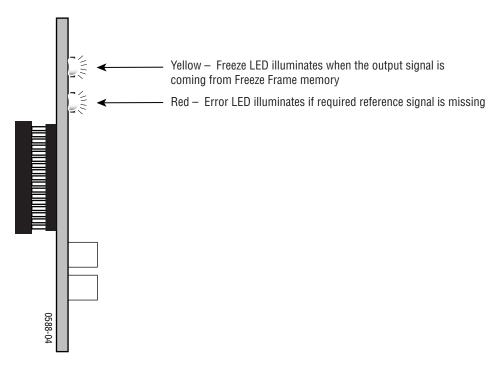


Figure 3. Indicator LEDs

Table 1. Error LED Status and Indicated Input Condition

Error LED (red)	Condition Reported	
0FF	Normal operation; a input reference signal is present †	
ON	No input reference signal is present	
Freeze LED (yellow)		
0FF	Output is active video.	
ON	Output is from 8900FSS memory.	

 $<sup>^\</sup>dagger$  If the reference does not match the selected video standard, the mismatch is reported to the host module. No action is reported on 8900FSS submodule indicators.

## **Configuration**

The configuration of the 8900FSS establishes the operation parameters shown in Table 2. The submodule configuration can be changed from factory defaults using the configuration switches on the host module. These switches are:

- Function Switch a function selection rotary switch (submodule functions are usually addressed by the second bank of selections on this switch).
- Toggle Switch a momentary toggle switch that actuates the selection when switched either up or down.

Refer to the instruction manual for the host module for configuration instructions.

Function Switch	Toggle Switch Up	Toggle Switch Down	Function	Description
0	Video	Reference †	Lock Source	Selecting Video forces delay mode even if a reference signal is present.
1	currently not used			
2	+	_	Horizontal Phase	Provides synchronizer phase adjustment in clock increments.
3	+	_	Vertical Phase	Provides synchronizer phase adjustment in full line increments
4	Manual <sup>†</sup>	Auto	Freeze Recognition	Selecting Auto stores the last field in the frame synchronizer to output if the input video is lost or corrupted.
5	Off †	On	Freeze Manual	Enables/Disables manual selection of Freeze Mode according to positions 6 and 7.
6	Frame <sup>†</sup>	Field	Freeze Mode	Select between Frame and Field.
7	Field 1 <sup>†</sup>	Field 2	Freeze Field	Select between Field 1 and Field 2.
8	Last Field <sup>†</sup>	Black	Freeze Signal	Selects the freeze output signal if Auto or manual freeze is activated.

Table 2. Frame Sync Configuration

## **Remote Configuration and Monitoring**

currently not used

The 8900FSS is designed to operate in 8900TX, TF or TFN frame versions that support GUI-based configuration and monitoring. A PROM upgrade on the host module may be required to activate frame bus communication if the module is moved from a non-networking frame to a networking frame.

<sup>9,</sup> A-F cu
† Default setting.

## **Specifications**

Table 3. 8900FSS Specifications

Parameter	Value	
Input Signal		
Туре	10-bit parallel 4:2:2 component video	
Signal level	C-MOS	
Setup data to clock	> 3 ns	
Hold data to clock	> 2 ns	
Output Signal		
Туре	10-bit parallel 4:2:2 component video	
Signal level	C-MOS	
Propagation delay to clock	< 8 ns	
Jitter <sup>†</sup>	Conforms to SMPTE17.12/002 <400 ps above 1 kHz	
Reference Signal		
Number of references	2	
Signal type	Black Burst Separate input assigned for SMPTE170M (525-line) and CCIR624 (625-line) input signal.	
Signal level	Sync: 300 mV p-p ±6 dB	
Input DC level	0V ±3V	
Input Impedance	75 Ω jumper terminated	
Connector type	75 <b>Ω</b> BNC on 8900 frame	
Return loss	> 40 dB to 5 MHz	
RMS signal-to-noise ratio	> 40 dB to 5 MHz required	
Performance		
Minimum delay	35 clock cycles	
Maximum delay	1 video frame	
Delay resolution	1 clock period = 37 ns	
Delay increments	1 clock = 37 ns 1 line = 1 full video line	
Reference to video timing relationship	No phase lock required	
Module		
Size	5 in. (127 mm) x 2.7in. (68.58 mm)	
Weight	2 oz	
Power consumption	< 2.0 W from +5 V, < 0.5 W from -5 V	
Environmental		
Temperature range	0 to 45°C ambient	
Relative humidity	0 to 90% non-condensing	
netative numbers	o to oo /o non conditioning	

<sup>†</sup> Measured in serialized output signal

#### **Service**

The 8900FSS and its host module make extensive use of surface-mount technology and programmed parts to achieve compact size and adherence to demanding technical specifications. Circuit modules should not be serviced in the field.

If your module is not operating correctly, proceed as follows:

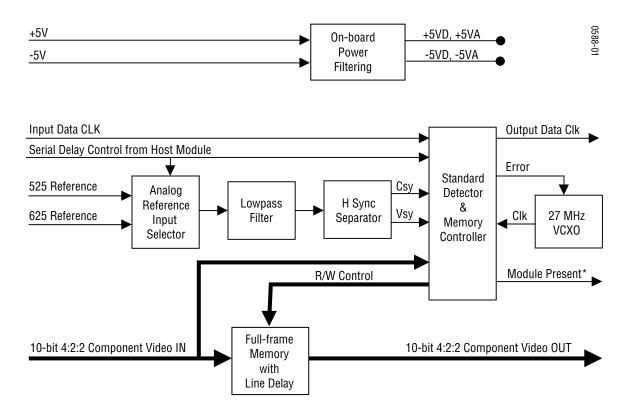
- Check frame and module power and signal present LEDs.
- Check for presence and quality of main input and reference signals.
- Verify that source equipment is operating correctly.
- Check cable connections.
- Check output connections for correct I/O mapping (correct input connector is used for the corresponding channel output).

If the module is still not operating correctly, replace it with a known good spare and return the faulty module to a designated Grass Valley repair depot. Call your Grass Valley representative for depot location.

Refer to the *Contacting Grass Valley Group* at the front of this document for the Grass Valley Customer Service Information number.

## **Functional Description**

Refer to the block diagram in Figure 4 while reading the following functional description.



<sup>\*</sup>The main Host module (DEC, ENC) automatically recognizes the attachment of the frame synchronizer submodule.

NOTE: All connections are made through the two 40-pin mainboard-to-subboard connector.

Figure 4. 8900FSS Frame Synchronizer Submodule Block Diagram

#### **Analog Reference Input Selector**

The analog reference video signals are connected to a high input impedance multiplexer that selects the appropriate input source. A removable jumper enables a loop-through input with proper return loss performance.

In the analog section the DC black level is not restored and therefore must be  $0~V\pm3~V$ . The overall video gain must be within  $\pm6~dB$  range of the nominal 1~V~p-p level.

#### **Low Pass Filter and H Sync Separator**

In the lowpass filter the signal is filtered and the subcarrier is trapped to prevent malfunctioning of the horizontal sync separator if a highly saturated reference signal (other than black-burst) is used.

The sync separator works over a wide  $\pm 6$  dB range and outputs a 50% sliced composite signal with low APL (average picture level) jitter.

#### **Standard Detector and Memory Controller**

Upon power up, the host module's microcontroller configures the onboard FPGA (field programmable gate array) by loading the firmware and the serial delay information according to the last stored user adjustments. The user adjustable parameters are input through a multifunction rotary switch and toggle switch combination interface that is part of the Host module. All the functions are remote read/write-able through the serial control interface.

#### **Full-frame Memory**

The submodule provides memory to hold a full frame of 525 or 625 video with additional auxiliary data. It is configured to be fully transparent to the 4:2:2 component data stream with a minimum latency of 35 clock cycles.

#### **Power Filtering**

The input +5V and –5V is filtered in multiple stages to isolate noise from the sensitive analog timing circuits and to minimize crosstalk and output jitter.

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